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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,320	08/30/2001	Travis Swanson	MIC-17	8733

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 06/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,320	SWANSON, TRAVIS	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,18-20 and 22-37* is/are rejected.

7)☒ Claim(s) *1,16,17,21,28 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 28 and 37 are objected to because of the following informalities:

The claims recite the limitation "subplurality of said pins". Although it is not unclear as to what it means, subplurality is not a word that is defined either in a dictionary or the specification. It is suggested that the limitation "subplurality of said pins" be substituted with a limitation that uses terms that are well defined, for example, "subset of said pins" or " at least one of said pins".

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 – 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 recites the limitation "one said pin" in line 6. There is insufficient antecedent basis for this limitation in the claim. Changing the limitation to "one of said pins" would overcome this rejection.

5. Claims 2 – 7 are rejected for including the deficiency of the parent claim as noted above.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 2, 6, 7, 13, 14, 23, 24, 25, 28, 30 – 33 and 35 – 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Ajanovic (US Patent No. 6,298,426).

8. With respect to claims 1, 6, 7, 13, 23 – 25, 27, 31, 33, 35 and 36, Ajanovic discloses a memory controller (figure 2) comprising:

at least one output pin;

a multiplexer (figure 4B, 402B) having two inputs, a control input, and an output coupled to said output pin;

a chip select signal (figure 4B,RAS7-6/CS7-6 signal, see also col. 7, lines 49 – 50) coupled to one of said two inputs;

a control signal (figure 4B, MA3-2 signal) coupled to the other one of said two inputs; and

a signal coupled (figure 4B, CFGAB signal) to said control input that selects one of said chip select signal and said control signal based on a type of memory (col. 4, lines 16 – 22, 55 –

58, col. 5, lines 41 – 42, col. 7, lines 18 – 22, the CKE signal, which depends on the type of memory, controls the CFGAB signal which in turn selects the multiplexed signal to output).

9. With respect to claims 28, 30 and 37, the difference between these claims and the above claims is the central processing unit. Ajanovic discloses a CPU (figure 1, 100, 101).

10. With respect to claims 2 and 14, the type of memory is buffered memory (figure 5).

11. Claims 1, 3, 4, 8, 10, 18, 20, 26, 29, 32 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Mehta *et al.* (US Patent No. 6,681,301, hereinafter "Mehta").

12. With respect to claims 1, 4, 8, 18, 26, 32 and 34, Mehta discloses a memory controller (claim 1) comprising:

at least one output pin (figure 3 and 3, 241, see also col. 12, lines 64 – 67);

multiplexer means having two inputs, a control input, and an output coupled to said output pin (claim 1, col. 13, lines 18 – 21);

a clock signal (data strobe signal, see also figures 4 and 5) coupled to one of said two inputs;

a control signal (data mask signal) coupled to the other one of said two inputs; and

means coupled to said control input for selecting one of said clock signal and said control signal based on a type of memory (col. 13, lines 9 – 15, 22 – 26).

13. With respect to claim 29, the difference between this claim and the above claims is the central processing unit. Metah discloses a CPU (figure 1).

14. With respect to claims 3, 10 and 20, the type of memory is unbuffered memory (col. 8, lines 4 – 5).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 5, 9, 11, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta in view of Gillingham *et al.* (US Patent Application No. 2001/0047450, hereinafter "Gillingham").

17. With respect to claims 5, 11, and 22, Mehta discloses all of the limitation of the parent claims 1, 8, and 18 as discussed above. However, Mehta does not specifically disclose that the clock signal is a differential clock signal. On the other hand, Gillingham discloses a memory system that uses a differential clock signal (page 6, paragraph 79).

It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham and Mehta before him at the time the invention was made, to use the differential

clock signal teachings of the memory system of Gillingham in the memory system of Mehta, in order to eliminate sensitivity of the clock path to a reference voltage variations and common mode noise throughout the system (Gillingham, page 6, paragraph 79).

18. With respect to claims 9 and 19, Mehta disclose all of the limitations of the parent claims 8 and 18 as discussed above. However, Mehta does not specifically disclose that the memory can be of buffered type. On the other hand, Gillingham discloses a system where the memory controller makes all timing adjustments so that both buffered and unbuffered types of memory modules can be used in the same system (Gillingham, page 9, paragraph 104).

It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham and Mehta before him at the time the invention was made, to use the timing adjustment teachings that allows the use of buffered and unbuffered memory system teachings of Gillingham in the memory system of Mehta, in order to increase bandwidth with no additional drawbacks to the system (Gillingham, page 9, paragraph 104). One of the advantages of Gillingham's invention, among others (see page 3, paragraphs 23 – 28), is that the clock travels the same distance as data and do not limit overall bus performance (page 3, paragraph 26). One skilled in the art would also be motivated to combine the teachings, because this combination has the additional advantage of increased variety of memory types that can be used in the system while maintaining constant timing between all memories. This additional flexibility provides one skilled in the art an additional degree of freedom when designing a memory system.

19. Claims 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic in view of Gillingham.

20. With respect to claim 12, Ajanovic discloses a method of providing more than one function for an output pin of a memory controller, said method comprising:

providing a control signal within said memory controller (figure 4B, RAS7-6/CS7-6);

selecting within said memory controller one of said clock signal and said control signal (figure 4B,RAS7-6/CS7-6 signal, see also col. 7, lines 49 – 50), based on a type of memory wherein said control signal is a chip select signal (col. 4, lines 16 – 22, 55 – 58, col. 5, lines 41 – 42, col. 7, lines 18 – 22, see also rejection of claim 1 above, also note that this limitation only requires that one of the two signals be selected and does not require that the selection be made between the two said signals); and

coupling said selected signal to said output pin.

However, Ajanovic does not specifically disclose the step of providing a clock signal within said memory controller. On the other hand, Gillingham discloses a method that provides a clock signal within the memory controller (figure 12, 165, clk).

It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham and Ajanovic before him at the time the invention was made, to use Gillingham's teaching to provide a clock signal within the memory controller in the memory controller of Mehta so that all of the timing adjustments can be made by the controller (Gillingham, page 9, paragraph 104). This allows the use of buffered and unbuffered memory in the same system and

achieve consistent timing between all memories. Gillingham's teachings increase the bandwidth with no additional drawbacks to the system (page 9, paragraph 104).

21. With respect to claim 15, Ajanovic discloses all of the limitations of the parent claim 13 as discussed above. However, Ajanovic does not specifically disclose that the memory is of unbuffered type. On the other hand, Gillingham discloses a system where the memory controller makes all timing adjustments so that both buffered and unbuffered types of memory modules can be used in the same system.

It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham and Mehta before him at the time the invention was made, to use the timing adjustment teachings that allows the use of buffered and unbuffered memory system teachings of Gillingham in the memory system of Mehta, in order to increase bandwidth with no additional drawbacks to the system (Gillingham, page 9, paragraph 104). This combination has the additional advantage of increased variety of memory types that can be used in the system while maintaining constant timing between all memories. This additional flexibility provides one skilled in the art an additional degree of freedom when designing a memory system.

Allowable Subject Matter

22. Claims 16, 17, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Olarig et al. (US Patent No. 6,530,007), Stolt et al. (Us Patent No. 5,893,136) and Begun et al. (Us Patent No. 5,375,084) other memory controllers that can be reconfigured to provide different functionalities to an output pin based on the memory type. Cowell (US Patent No. 5,860,134), Matsuda (US Patent Application Pub. No. US2001/0054135), Bowater et al. (US Patent No. 5,301,278) and Cho et al. (US Patent No. 6,625,685) disclose other memory controllers that can be configured to work with different types of memory modules.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc
May 21, 2004

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